

RS8228/M28228

Errata

HEC Error Insertion Failure

The insert HEC error function, (bit 4 of the CGEN register, 0x08) may not error the HEC when set high. This is due to an internal counter that inadvertently clears before reaching a count of 53. The failure occurs approximately 60% of the time.

UTOPIA FIFO may lock up if an overflow is allowed to occur.

The Rx UTOPIA FIFO may lock up if an overflow occurs. An Rx FIFO Overflow may occur randomly when there is a step change in bandwidth caused by a link going down and up, port configuration change, or some other condition. In this occurrence, the RxOvfl bit in register 0x02E (port0) is set to a logical one which indicates that a Receive FIFO Overflow condition occurred in the receive UTOPIA FIFO. This bit will be stuck high when the FIFO is locked up and will be unable to transfer data. Similarly, the transmit side may lockup. The transmit side may lockup if the Transmit FIFO's are allowed to overflow. Generally, this indicates that a violation of the UTOPIA standard has occurred.

Workaround:

To clear the lockup condition a FIFO reset should be executed by setting and clearing the appropriate FIFO reset bit in address 0x00D (port0). If this doesn't clear the condition, reset the port using the Port Logic Reset bit. If this doesn't clear the condition, then software will need to set and clear the Port Master Reset bit, and reconfigure the port. If this doesn't clear the condition, then software will need to set then clear the Device Master Reset bit and reconfigure the device.

Clocks must be present during Reset.

The RS8228 is composed of 5 primary blocks: Microprocessor interface, TX UTOPIA, RX UTOPIA, TX Port, and RX Port (the Port blocks are duplicated 8 times; once for each port). Each block uses it's own clock during the device Reset. To ensure proper operation, ALL clocks must be present during the Reset sequence and should remain active for a minimum of 3 clock cycles after the Reset is cleared. This applies to all methods and levels of Reset: Hardware Reset using the RESET* pin, as well as software methods that use the Device Master, Device Logic, Port Master, or Port Logic control bits.

The Port clocks may be shut down or 'gapped' after the reset is finished.

De-asserting UTOPIA Rx Enable during Start of Cell.

De-asserting the UTOPIA Rx Enable input, (UrxEnb*, pin Y14), while the SOC output is active may result in unpredictable behavior for that port.

This should not have a major impact on customer designs since almost all UTOPIA Masters will transfer the entire cell before de-asserting the enable line.